Towards implementation of a Time-Sensitive Networking switch

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ABSTRACT

Time-Sensitive Networking (TSN) is emerging as an industry standard to support URLLC applications such as Telesurgery at the Data Link layer. The IEEE standard 802.1 TSN proposes several traffic schedulers and shapers for TSN, of which 802.1Qbv Time-Aware Shaper (TAS) provides best-in-class performance in simulations. Switches in the market supporting TSN features are very few and they do not offer programmability. We exploit the flexibility in dataplane programming provided by P4 to implement a TAS on a P4-compliant SmartNIC (Netronome Agilio CX).

KEYWORDS

TSN, SDN, P4, FPGA

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1 INTRODUCTION

Success in using networks to handle remote applications has led to new applications involving haptic feedback which use a network for bilateral communication. Telesurgery and remote-driving are a couple of examples which demand low and bounded latency, of the order of ten milliseconds, and high reliability (99.999 %).

Advent of SDN has enabled logical separation of the network's control and data planes. Control plane algorithms can now be written with software such as Python, and data plane algorithms can be described using an open-source network-domain programming language called P4. With the introduction of reconfigurable programmable hardware, researchers have a robust infrastructure to test real-world performance of their custom applications.

IEEE 802.1 TSN, a Layer-2 technology, is used to provide determinism on Ethernet which is traditionally a best-effort technology. To acheive low latencies of the order of ten milliseconds, for scheduled traffic, the TSN standard proposes 802.1Qbv Time-Aware Shaper (TAS). TAS queues incoming packets into multiple egress queues of a port, and implements a time schedule with a gate control mechanism to allow specific queues to trasmit at specified intervals. The standard provides a mechanism for closing and opening of gates and leaves scheduling of opening/closing the gates open to the research community. We focus on implementing 802.1Qbv TAS with a custom scheduling algorithm to acheive the latency values promised by the standard.

2 RELATED WORK

Tokmakov et al. [1] have implemented traffic management on software switches such as BmV2.

3 METHODOLOGY AND NEXT STEPS

We are building a TSN switch and demonstrate 802.1Qbv TAS as a step towards it. Such switches require support of multiple queues and implementation of custom scheduling/shaping algorithms.

A switch's dataplane behaviour involves parsing incoming packets, applying match-action tables and putting the packets back together and assigning these to egress queues. This is called Traffic Classification. Next, the switch implements a scheduling strategy for dequeuing packets. This is called Traffic Scheduling and Shaping.

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P4 can describe Traffic Classification. However, Traffic Scheduling/Shaping requires proprietary hardware tools for programming. We procured Netronome Agilio CX that offers native support for P4. The Netronome's firmware can be programmed using Micro-C language and we can potentially use this to program the scheduler to build the Gate Control Logic. We have succeeded in getting timestamps from the Netronome, which we will use to implement our scheduler.

4 EVALUATION

We use a desktop PC which acts as a host and is connected to the TSN switch through Ethernet cables. It generates, transmits and receives packets. A ping from the host to the switch and back will provide latency numbers.

REFERENCES

[1] Kamil Tokmakov, Mitalee Sarker, Jörg Domaschka, and Stefan Wesner. 2019. A case for data centre traffic management on software programmable ethernet switches. In *2019 IEEE 8th International Conference on Cloud Networking (CloudNet)*. IEEE, 1–6.